WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a lower-layer interconnection;

forming a protective film on a surface of the lower-layer interconnection;

forming a multilayer-structured film by stacking a first porous film, a first non-porous film, a second porous film, and a second non-porous film on a surface of the protective film in this order;

forming a via hole in the first porous film and the first non-porous film, and forming an interconnect trench communicating with the via hole in the second porous film and the second non-porous film, by dry etching the multilayer-structured film using a resist mask;

removing the resist mask;

removing the protective film exposed at a bottom of the via hole after removing the resist mask; and

forming an upper-layer interconnection of dual damascene structure by embedding an interconnect material in the via hole and the interconnect trench, the upper-layer interconnection being connected to the lower-layer interconnection,

wherein for the first non-porous film, used is a multilayer film including at least two layers in which a first layer, which is located close to the first porous film, is made of a material that has a high etching selectivity ratio relative

to the protective film, and a second layer, which is located closer to the second porous film than the first layer is, is made of a material that has a high etching selectivity ratio relative to the resist mask and the second porous film.

2. The method according to claim 1, wherein the first non-porous film is formed by stacking a lower layer and an upper layer thereon, the upper layer is made of a material which has a high etching selectivity ratio relative to the second porous film and the resist mask, and the lower layer is made of a material which has a high etching selectivity ratio relative to the protective film.

3. The method according to claim 1, wherein the first non-porous film is formed by stacking two or more layers including at least a lower layer and an upper layer, the upper layer is made of a material which has a high etching selectivity ratio relative to the second porous film, the lower layer is made of a material which has a high etching selectivity ratio relative to the upper layer, and any one layer of the multilayer film including two or more layers is made of a material which has a high etching selectivity ratio relative to the protective film.

4. A method of manufacturing a semiconductor device, comprising:

forming a lower-layer interconnection;

forming a protective film on a surface of the lower-layer

interconnection;

forming a multilayer-structured film by stacking a first porous film, a first non-porous film, a second porous film, and a second non-porous film on a surface of the protective film in this order;

forming a via hole in the first porous film and the first non-porous film, and forming an interconnect trench communicating with the via hole in the second porous film and the second non-porous film, by dry etching the multilayer-structured film using a resist mask;

removing the protective film exposed at a bottom of the via hole;

removing the resist mask after removing the protective film; and

forming an upper-layer interconnection of dual damascene structure by embedding an interconnect material in the via hole and the interconnect trench, upper-layer interconnection being connected to the lower-layer interconnection,

wherein for the first non-porous film, used is a multilayer film including at least two layers in which a first layer, which is located close to the first porous film, is made of a material that has a high etching selectivity ratio relative to the resist mask, and a second layer, which is located closer to the second porous film than the first layer is, is made of a material that has a high etching selectivity ratio relative to the protective film and the second porous film.

5. The method according to claim 4, wherein the first non-porous film is formed by stacking a lower layer and an upper layer thereon, the upper layer is made of a material which has a high etching selectivity ratio relative to the protective film and the second porous film, and the lower layer is made of a material which has a high etching selectivity ratio relative to the resist mask.

6. The method according to claim 4, wherein the first non-porous film is formed by stacking two or more layers including at least a lower layer and an upper layer, the upper layer is made of a material which has a high etching selectivity ratio relative to the second porous film, the lower layer is made of a material which has a high etching selectivity ratio relative to the upper layer, and any one layer of the multilayer film including two or more layers is made of a material which has a high etching selectivity ratio relative to the protective film.

7. A semiconductor device, comprising:

a lower-layer interconnection formed on a semiconductor substrate with an insulating film interposed therebetween;

a protective film formed on a surface of the insulating film, including on the lower-layer interconnection;

a multilayer-structured film formed by stacking at least a first porous film, a first non-porous film, and a second porous film on a surface of the protective film in this order; and

an upper-layer interconnection of dual damascene structure formed in the protective film and the multilayer-structured film, the upper-layer interconnection including a via plug part connected to the lower-layer interconnection and an interconnect part connected to the via plug part with a boundary of the first non-porous film,

wherein the first non-porous film is a multilayer film including at least two layers, the first non-porous film including any one of the layers is made of a material which has a high etching selectivity ratio relative to the protective film, a layer located close to the first porous film is made of a material which has a high etching selectivity ratio relative to a layer located close to the second porous film, and a layer located close to the second porous film is made of a material which has a high etching selectivity ratio relative to the second porous film.

8. The semiconductor device according to claim 7, wherein the first non-porous film has a multilayer structure with a lower layer and an upper layer stacked thereon, and the lower layer is made of a material which has a high etching selectivity ratio relative to the protective film.

9. The semiconductor device according to claim 8, wherein the lower layer included in the first non-porous film is a polyarylene ether film.

10. The semiconductor device according to claim 9, wherein the upper layer included in the first non-porous film is any

one of SiCH film, SiCN film, SiCO film, SiN film, organic siloxane film, and inorganic siloxane film.

11. The semiconductor device according to claim 7, wherein the first non-porous film has a multilayer structure with a lower layer and an upper layer stacked thereon, and the upper layer is made of a material which has a high etching selectivity ratio relative to the protective film.

12. The semiconductor device according to claim 11, wherein the upper layer included in the first non-porous film is a polyarylene ether film.

13. The semiconductor device according to claim 12, wherein the lower layer included in the first non-porous film is any one of SiCH film, SiCN film, SiCO film, SiN film, organic siloxane film, and inorganic siloxane film.

14. The semiconductor device according to claim 7, wherein among the layers in the multilayer film constituting the first non-porous film, the layer made of the material which has a high etching selectivity ratio relative to the protective film, is a polyarylene ether film.

15. The semiconductor device according to claim 7, wherein the protective film is any one of SiCH film, SiCN film, SiCO film, and SiN film.

16. The semiconductor device according to claim 7, wherein at least one of the first and second porous films is any one of porous organic siloxane film and porous inorganic siloxane film.

17. The semiconductor device according to claim 7, wherein at least one of the first and second porous films is porous polyarylene ether film.

18. The semiconductor device according to claim 7, wherein the first non-porous film is thinner than the protective film.

19. The semiconductor device according to claim 7, wherein the multilayer-structured film has a multilayer structure in which the first porous film, the first non-porous film, the second porous film, and a second non-porous film are stacked in this order.

20. The semiconductor device according to claim 19, wherein the second non-porous film is any one of organic siloxane film and inorganic siloxane film.